RM-N95

SMARC 2.2 CPU Module with NXP i.MX95 Cortex-A55 and Neutron NPU

User's Manual

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CE

The product described in this manual complies with all applicable European Union (CE) directives if it has a CE marking. For systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cables and cabling techniques.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer’s instructions, may cause harmful interference to radio communications.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE

This product complies with RoHS 2 restrictions, which prohibit the use of certain hazardous substances in electrical and electronic equipment. The following substances must not exceed the specified concentrations:

- Hexavalent chromium: 1,000 ppm
- Poly-brominated biphenyls (PBBs): 1,000 ppm
- Poly-brominated diphenyl ethers (PBDEs): 1,000 ppm
- Cadmium: 100 ppm
- Mercury: 1,000 ppm
- Lead: 1,000 ppm
- Bis(2-ethylhexyl) phthalate (DEHP): 1,000 ppm
- Butyl benzyl phthalate (BBP): 1,000 ppm
- Dibutyl phthalate (DBP): 1,000 ppm
- Diisobutyl phthalate (DIBP): 1,000 ppm

Important Handling and Safety Information

Carefully read the following handling and integration safety information before installing or operating the RM-N95 module.

System Integration Notice

- The RM-N95 module is intended for integration into a custom or standard SMARC 2.2 carrier board.
- Do not power or operate the module independently. Always ensure the carrier board design complies with SMARC electrical, mechanical, and thermal specifications.

Handling Precautions

- Handle the module only in an ESD-protected environment.
- Avoid mechanical shock, bending, or flexing of the PCB.
- Store the module in an anti-static bag when not in use.
- Avoid touching connector fingers or exposed components.
- The RM-N95 is a sealed PCB assembly; do not disassemble, rework, or modify components unless authorized by the manufacturer.

Power Safety

- The supply voltage to the module must follow SMARC 2.2 specifications (typically 3.3 V and/or 5 V provided from the carrier).
- Always verify correct polarity and stable power rails before power-on.
- Do not insert or remove the module while the carrier board is powered.

Warranty Policy

IBASE warrants its RM-N95 SMARC module against defects in materials and workmanship for a period of 24 months from the date of shipment.
If the shipment date is unavailable, the serial number will be used to determine the approximate manufacturing date.

Third-party components supplied with or integrated into the module (e.g., memory, storage devices, power adapters, or display panels)
carry a 12-month warranty, or as defined by their respective manufacturers.

The warranty does not apply to products that have been:

- Damaged by accident, misuse, or improper installation
- Modified, repaired, or reworked without IBASE authorization
- Operated outside of rated electrical or environmental conditions

Out-of-warranty repairs may be performed at customer expense, including shipping and handling costs.

Technical Support & RMA Service

For product updates, technical assistance, or documentation, please visit the IBASE website: https://www.ibase.com.tw

If technical support is required, please contact your IBASE representative and provide the following information:

- Product model name and serial number
- Description of the issue and steps to reproduce it
- Firmware or operating system version
- Connected peripherals and configuration details
- Any error logs, console output, or screenshots (if available)

For repair or replacement service, please obtain a Return Material Authorization (RMA) number through the IBASE website before returning any product.

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Chapter 1
General Information

The information provided in this chapter includes:

- Introduction
- Features
- Specifications
- Product View
- Dimensions

1.1 Introduction

The RM-N95 is a SMARC 2.2 Computer-on-Module (COM) based on the NXP® i.MX95 processor, featuring six Arm Cortex-A55 cores with integrated Cortex-M7 and Cortex-M33 cores for real-time and secure processing. It includes a Neutron™ NPU delivering up to 2.0 TOPS for AI acceleration. The module integrates 8 GB LPDDR5 memory, 16 GB eMMC storage (expandable to 256 GB), and supports HDMI, dual-channel LVDS, optional 4-lane MIPI-DSI, 2x GbE, 1x 10GbE, USB 3.0 Type-C, USB 2.0, and dual PCIe® 3.0 interfaces. Designed for industrial applications, the RM-N95 complies with the SMARC 2.2 (82 × 50 mm) form factor, is validated with Yocto, and supports operating temperatures from −40 °C to +85 °C.

1.2 Features

- 6x Arm Cortex-A55, 1x Cortex-M33 and 1x Cortex-M7
- Neutron NPU 2.0 TOPS
- Onboard 8GB LPDDR5, 16GB eMMC (expandable to 256GB)
- 1x HDMI, 1x Dual-channel LVDS, 1x 4-lane MIPI-DSI (optional)
- 1x 10GbE + 2x GbE, 1x USB 3.0 Type-C, 1x USB 2.0, 2x PCIe 3.0 x 1-lane
- CRA / TPM Security, EdgeLock Secure Enclave
- Validated with Yocto 5.0
- Wide-range operating temperature from -40°C to +85°C

1.3 Specifications

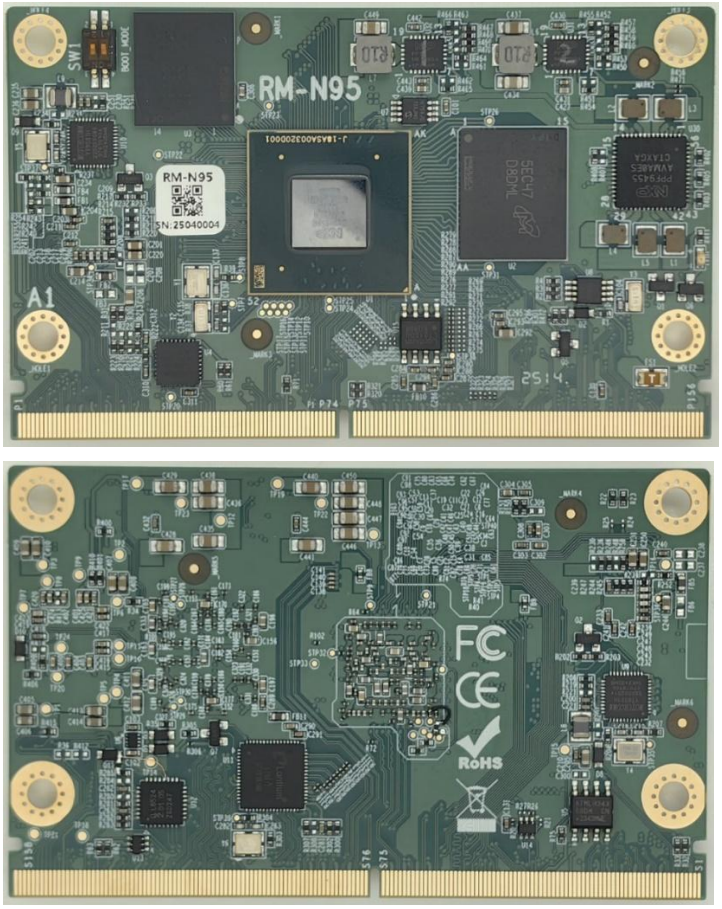
Product Name	RM-N95
Form Factor	SMARC 2.2 - 82 mm × 50 mm
Processor	NXP i.MX95 with Cortex-A55, six cores, 2.0 GHz (industrial grade); supports 64-bit Arm v8.2 architecture
System Memory	8GB LPDDR5 6400 MT/s onboard (optional 4 GB or 16 GB)
Flash Memory	16GB eMMC NAND Flash for O.S. (expandable up to 256GB) and 8 Kbit EEPROM for board information
Neural Processing Unit (NPU)	Up to 2.0 TOPS AI performance
Display	• 1x 4-lane MIPI-DSI (4Kp30 or 3840×1440p60, BOM selectable) • 1x 8-lane or 2x 4-lane LVDS (up to 1080p or 1920×1200 or dual 720P) • 1x HDMI interface (up to 4Kp30 or 3840×1440p60)
Video Codec	Decoder: H.265, H.264, 4Kp30 Encoder: H.265, H.264, 4Kp30
Graphics	Arm Mali-G310 V2 GPU; OpenGL® ES 3.2; Vulkan® 1.3; OpenCL 3.0
I/O Ports	
Audio Interface	2x I2S
LAN	1x 10GbE + 2x GbE
USB	• 1x USB 3.0 Type-C with PHY • 1x USB 2.0 with PHY
Image Capture	• 1x MIPI CSI-2 2-Lane (BOM selectable) • 1x MIPI CSI-2 4-Lane
Serial Interface	• 2x 4-wire UART and 2x 2-wire UART • 1x SPI interface • 1x XSPI interface
Media Interface	1x 4-bit high-speed SDIO
PCI-E	2x PCI-E 3.0 x1 lanes
SATA	N/A
GPIO	14x GPIO
I²C	4x I²C
CAN Bus	2x CAN FD
Others	• Security: CRA / TPM 2.0 • RTC: Yes • Watchdog timer: 1~6553s, power on/off 4s • 1x Green LED for power status
OS Support	Yocto 5.0 (other OS by request)
Certification	CE / FCC Class B

Dimensions	
PCB Dimensions	8-layer PCB Board: 82mm x 50mm (3.23” x 1.97”) Max component height -Top Side: 3.0mm -Bottom Side: 1.3mm Thickness: 1.2mm -Golden Finger: 45° chamfer (0.18mm)
Environment	
Operating Temperature	Operating: -40°C to +85°C (-40°F~185°F) (Industrial grade, with heat-sink) Storage: -40°C to 85°C(-40°F~185°F)
Relative Humidity	0 % to 90 % RH at 60° C (non-condensing)

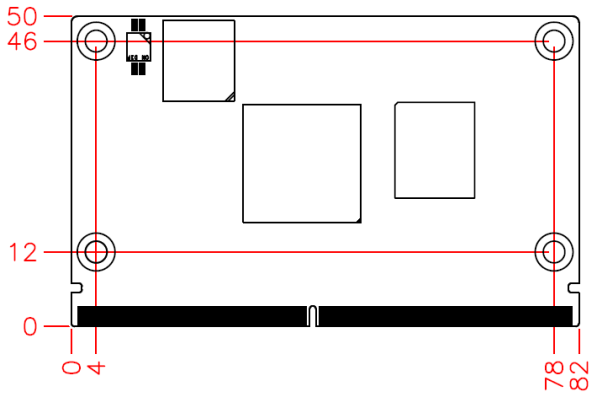
All specifications are subject to change without prior notice.

Ordering Information	
Model	Description
RM-N95	SMARC Module with NXP i.MX95 Cortex-A55, 8GB LPDDR5, 16GB eMMC

1.4 Product View



1.5 Dimensions



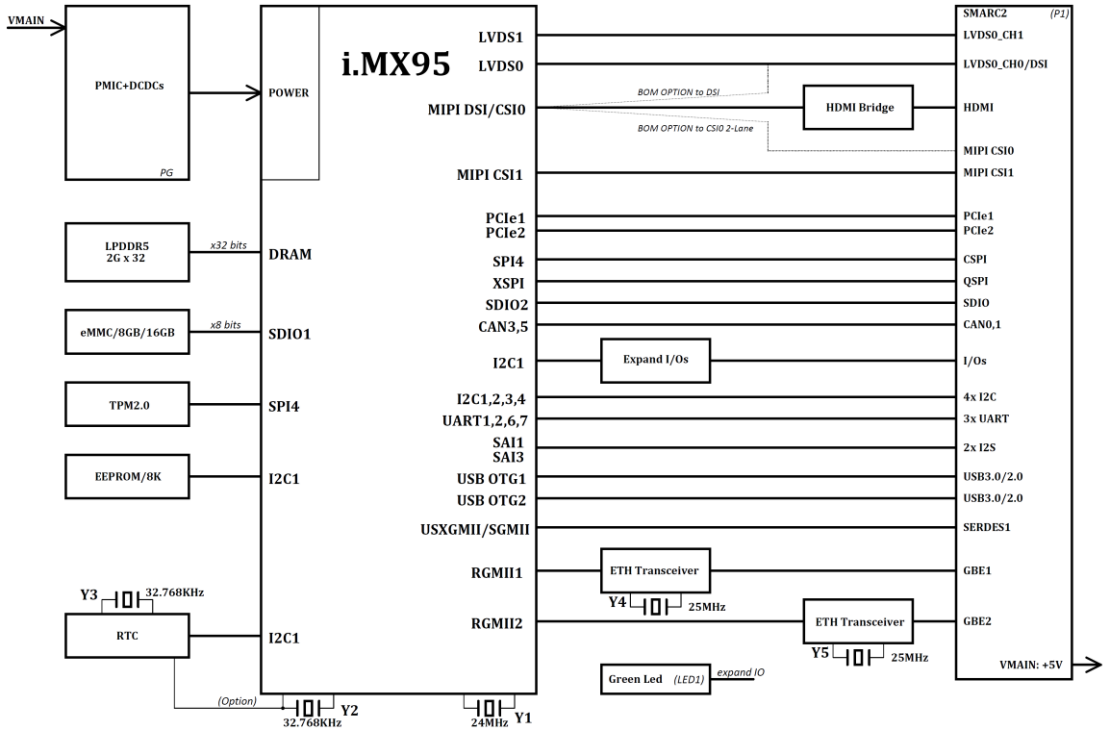
Unit: mm

Chapter 2
Hardware Configuration

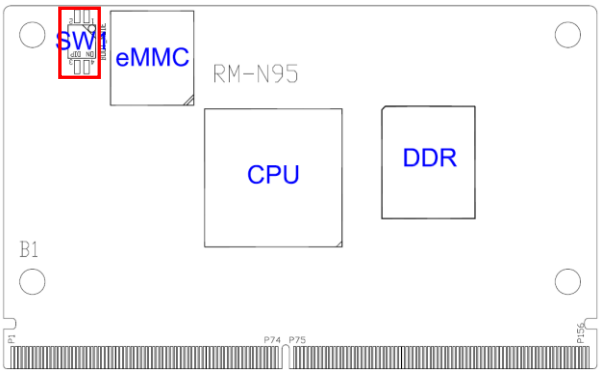
This section contains general information about:

- Block Diagram
- Boot Mode Selection
- Module Outline
- Carrier Board Connector PCB Footprint
- Module Pin Assignments
- Signal Direction and Type Definitions

2.1 Block Diagram



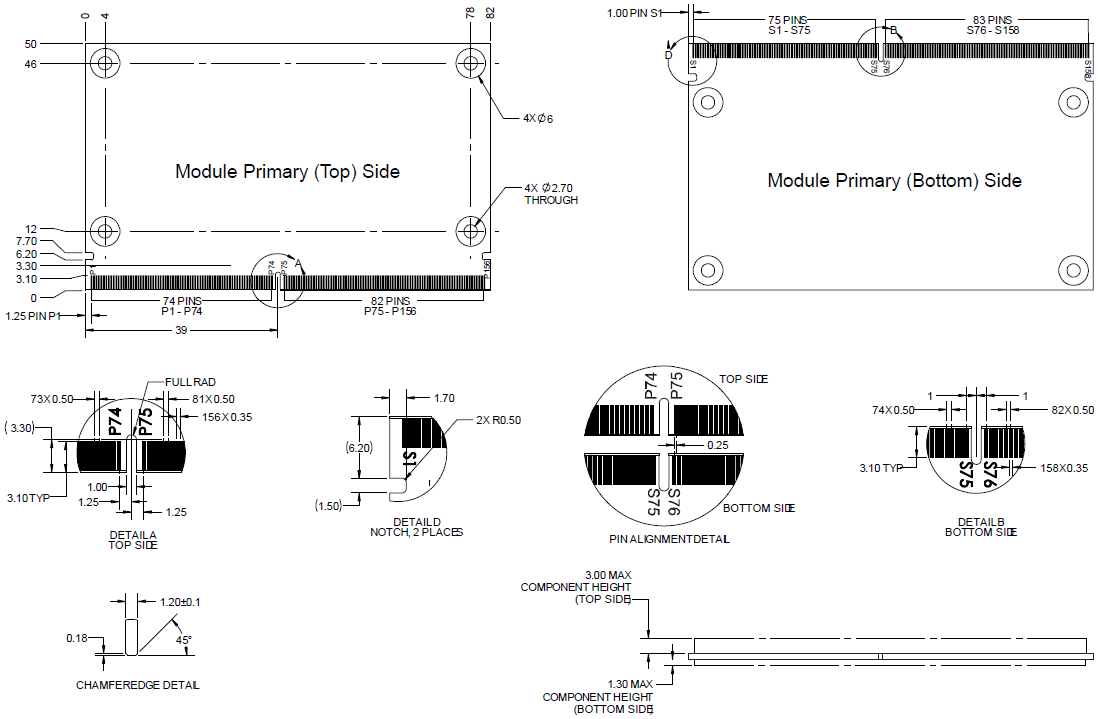
2.2 Boot Mode Selection



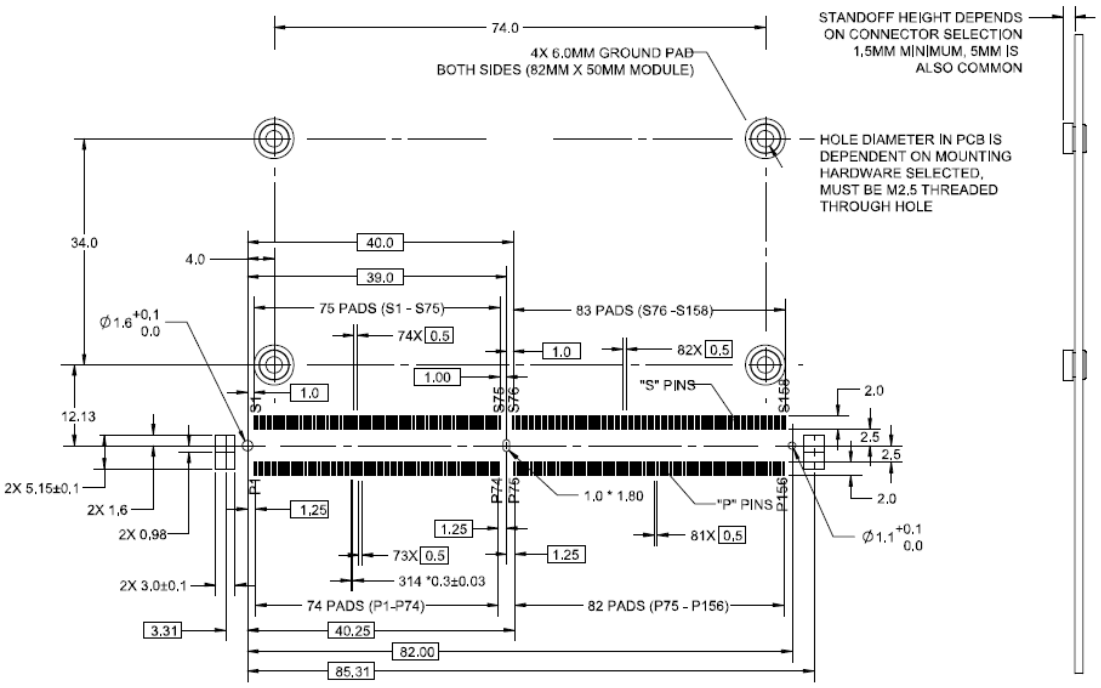
Mode	Signal Name	
	SW1_1–4	SW1_2–3
Normal Boot	ON	OFF
SD Boot	ON	ON
USB Download	OFF	ON

Note:
Edge-finger pin P123 (BOOT_MODE0) connect to SW1 2-3,
Edge-finger pin P124 (BOOT_MODE1) connect to SW1 1-4,
Edge-finger pin P125 (BOOT_MODE2) pull-down with 10K resistor.

2.3 Module Outline



2.4 Carrier Board Connector PCB Footprint



2.5 Module Pin Assignments

Pin	Assignment	Pin	Assignment
P1	SMB_ALT_B/GPIO5_06/BT_RESET	S1	I2C3_SCL
P2	GND	S2	I2C3_SDA
P3	CSI1_CKP	S3	GND
P4	CSI1_CKN	S4	NC
P5	ETH1_1588PPS_OUT	S5	I2C1_SCL
P6	ETH0_1588PPS_OUT	S6	CLKO1_CSI_MCLK
P7	CSI1_DP0	S7	I2C1_SDA
P8	CSI1_DN0	S8	CSI0_CKP
P9	GND	S9	CSI0_CKN
P10	CSI1_DP1	S10	GND
P11	CSI1_DN1	S11	CSI0_DP0
P12	GND	S12	CSI0_DN0
P13	CSI1_DP2	S13	GND
P14	CSI1_DN2	S14	CSI0_DP1
P15	GND	S15	CSI0_DN1
P16	CSI1_DP3	S16	GND
P17	CSI1_DN3	S17	GBE1_TRXP0
P18	GND	S18	GBE1_TRXN0
P19	GBE0_TRXN3	S19	GBE1_LED_10_100
P20	GBE0_TRXP3	S20	GBE1_TRXP1
P21	GBE0_LED_10_100	S21	GBE1_TRXN1
P22	GBE0_LED_1000	S22	GBE1_LED_1000
P23	GBE0_TRXN2	S23	GBE1_TRXP2
P24	GBE0_TRXP2	S24	GBE1_TRXN2
P25	GBE0_LED_ACT	S25	GND
P26	GBE0_TRXN1	S26	GBE1_TRXP3
P27	GBE0_TRXP1	S27	GBE1_TRXN3
P28	NC	S28	NC
P29	GBE0_TRXN0	S29	NC
P30	GBE0_TRXP0	S30	NC
P31	NC	S31	GBE1_LED_ACT
P32	GND	S32	NC
P33	NC	S33	NC
P34	SD2_CMD	S34	GND
P35	SD2_CD_B	S35	NC
P36	SD2_CLK	S36	NC
P37	SD2_RESET_B	S37	USB_OTG2_VBUS_DET
P38	GND	S38	AP_CODEC_MCLK
P39	SD2_DATA0	S39	SAI1_TXFS
P40	SD2_DATA1	S40	SAI1_TXD
P41	SD2_DATA2	S41	SAI1_RXD
P42	SD2_DATA3	S42	SAI1_TXC

Pin	Assignment	Pin	Assignment
P43	SPI4_SS0	S43	GPIO5_08/XSPI_DQS
P44	SPI4_SCLK	S44	NC
P45	SPI4_MOSI	S45	NC
P46	SPI4_MISO	S46	NC
P47	GND	S47	GND
P48	NC	S48	I2C3_SCL
P49	NC	S49	I2C3_SDA
P50	GND	S50	HDA_SAI3_TXFS
P51	NC	S51	HDA_SAI3_TXD
P52	NC	S52	HDA_SAI3_RXD
P53	GND	S53	HDA_SAI3_TXC
P54	GPIO5_10/XSPI_SS0	S54	SATA_ACT_B/GPIO3_20/SD3_CLK
P55	GPIO5_11/XSPI_SS1	S55	NC
P56	GPIO5_09/XSPI_SCLK	S56	GPIO5_02/XSPI_DATA2
P57	GPIO5_01/XSPI_DATA1	S57	GPIO5_03/XSPI_DATA3
P58	GPIO5_00/XSPI_DATA0	S58	GPIO5_07/XSPI_RST_B
P59	GND	S59	NC
P60	USB1_DP	S60	NC
P61	USB1_DN	S61	GND
P62	GPIO5_04/USBOTG1_OC_B	S62	USB2_TXP
P63	USB_OTG1_VBUS_DET	S63	USB2_TXN
P64	GPIO2_18/USBOTG1_ID	S64	GND
P65	NC	S65	USB2_RXP
P66	NC	S66	USB2_RXN
P67	NC	S67	GND
P68	GND	S68	USB2_DP
P69	NC	S69	USB2_DN
P70	NC	S70	GND
P71	GPIO5_05/USBOTG1_PWR	S71	USB1_TXP
P72	ENET_MDC	S72	USB1_TXN
P73	ENET_MDIO	S73	GND
P74	NC	S74	USB1_RXP
P75	GPIO3_30/PCIe1_RST_B	S75	USB1_RXN
P76	NC	S76	P20/PCIe2_RST_B
P77	PCIe2_CLKREQ_B	S77	P21/ETH_RST_B
P78	PCIe1_CLKREQ_B	S78	ETH_RX0_P
P79	GND	S79	ETH_RX0_N
P80	ETH_CLKIN_P	S80	GND
P81	ETH_CLKIN_N	S81	ETH_TX0_P
P82	GND	S82	ETH_TX0_N
P83	PCIe1_CLK_P	S83	GND
P84	PCIe1_CLK_N	S84	PCIe2_CLK_P
P85	GND	S85	PCIe2_CLK_N
P86	PCIe1_RX0_P	S86	GND

Pin	Assignment	Pin	Assignment
P87	PCIe1_RX0_N	S87	PCIe2_RX0_P
P88	GND	S88	PCIe2_RX0_N
P89	PCIe1_TX0_P	S89	GND
P90	PCIe1_TX0_N	S90	PCIe2_TX0_P
P91	GND	S91	PCIe2_TX0_N
P92	HDMI_TX2_P	S92	GND
P93	HDMI_TX2_N	S93	NC
P94	GND	S94	NC
P95	HDMI_TX1_P	S95	NC
P96	HDMI_TX1_N	S96	NC
P97	GND	S97	NC
P98	HDMI_TX0_P	S98	NC
P99	HDMI_TX0_N	S99	NC
P100	GND	S100	NC
P101	HDMI_TXC_P	S101	GND
P102	HDMI_TXC_N	S102	NC
P103	GND	S103	NC
P104	HDMI_HPD	S104	P07/USBOTG2_ID
P105	HDMI_CTRL_CK	S105	NC
P106	HDMI_CTRL_DAT	S106	NC
P107	HDMI_CEC_A	S107	GPIO1_08/LVDS_BL_PWEN
P108	P15/CSI0_PWEN_B	S108	LVDS1_CLK_P
P109	GPIO2_14/CSI1_PWEN_B	S109	LVDS1_CLK_N
P110	P14/CSI0_RST_B	S110	GND
P111	GPIO2_15/CSI1_RST_B	S111	LVDS1_TX0_P
P112	P13/HDA_RST_B/BT_H_WAKE_B	S112	LVDS1_TX0_N
P113	GPIO2_13/PWM3_OUT	S113	NC
P114	TACHIN/GPIO3_29/WIFI_REGON	S114	LVDS1_TX1_P
P115	P06/CODEC_INT_B	S115	LVDS1_TX1_N
P116	P05/WIFI_WAKE_B	S116	GPIO1_09/LVDS_EN
P117	P00/TP_INT_B	S117	LVDS1_TX2_P
P118	P11/TP_RST_B	S118	LVDS1_TX2_N
P119	P12/TP_EN_B	S119	GND
P120	GND	S120	LVDS1_TX3_P
P121	I2C4_SCL	S121	LVDS1_TX3_N
P122	I2C4_SDA	S122	GPIO4_28/LVDS_BL_PWM
P123	BOOT_MODE0	S123	P10_GPIO13
P124	BOOT_MODE1	S124	GND
P125	BOOT_MODE2	S125	DSI/LVDS0_TX0_P
P126	RESET_OUT_B	S126	DSI/LVDS0_TX0_N
P127	RESET_IN_B	S127	GPIO1_10/LCD_BL_PWEN
P128	ONOFF_B	S128	DSI/LVDS0_TX1_P
P129	UART6_TXD	S129	DSI/LVDS0_TX1_N
P130	UART6_RXD	S130	GND

Pin	Assignment	Pin	Assignment
P131	UART6_RTS	S131	DSI/LVDS0_TX2_P
P132	UART6_CTS	S132	DSI/LVDS0_TX2_N
P133	GND	S133	GPIO3_31/LCD_EN
P134	UART1_TXD	S134	DSI/LVDS0_CLK_P
P135	UART1_RXD	S135	DSI/LVDS0_CLK_N
P136	UART7_TXD	S136	GND
P137	UART7_RXD	S137	DSI/LVDS0_TX3_P
P138	UART7_CTS	S138	DSI/LVDS0_TX3_N
P139	UART7_RTS	S139	I2C4_SCL
P140	UART2_TXD	S140	I2C4_SDA
P141	UART2_RXD	S141	GPIO5_27/LCD_BL_PWM
P142	GND	S142	P16/GPIO12
P143	CAN3_TX	S143	GND
P144	CAN3_RX	S144	NC
P145	CAN5_TX	S145	WDOG1_OUTPUT_B
P146	CAN5_RX	S146	PCIe_WAKE_B/GPIO3_24/SD3_DATA2
P147	VMAIN	S147	LI_CELL
P148	VMAIN	S148	LID_B/GPIO3_21/SD3_CMD
P149	VMAIN	S149	SLEEP_B/GPIO3_25/SD3_DATA3
P150	VMAIN	S150	VIN_PWR_BAD_B
P151	VMAIN	S151	CHARGING_B/GPIO3_22/SD3_DATA0
P152	VMAIN	S152	CHR_PRSNT_B/GPIO3_28/BT_WAKE_B
P153	VMAIN	S153	SYSTEM_STBY_B
P154	VMAIN	S154	P23/PWR_ON
P155	VMAIN	S155	F_RECOV_B/GPIO3_23/SD3_DATA1
P156	VMAIN	S156	BATLOW_B/GPIO2_12/WIFI_CK
		S157	NC
		S158	GND

2.6 Signal Direction and Type Definitions

The following table lists the signal direction and type definitions for each pin. Key abbreviations: I = Input, O = Output, I/O = Bidirectional, CMOS = CMOS logic, D-PHY = MIPI D-PHY, GBE MDI = Gigabit Ethernet MDI.

Pin	Signal Name	Description	I/O	I/O Level
P1	SMB_ALT_B/GPIO5_06/BT_RESET	SMBus Interrupt Signal	I	CMOS 1.8V
P3/P4	CSI1_CKP / CSI1_CKN	CSI1 differential clock input	I	D-PHY
P5	ETH1_1588PPS_OUT	IEEE 1588 Trigger Signal	O	CMOS 1.8V
P7/P8	CSI1_DP0 / CSI1_DN0	CSI1 differential input	I	D-PHY
P10/P11	CSI1_DP1 / CSI1_DN1	CSI1 differential input	I	D-PHY
P13/P14	CSI1_DP2 / CSI1_DN2	CSI1 differential input	I	D-PHY
P16/P17	CSI1_DP3 / CSI1_DN3	CSI1 differential input	I	D-PHY
P19/P20	GBE0_TRXN3 / TRXP3	GBE0 Differential Pair Signals	I/O	GBE MDI
P21	GBE0_LED_10_100	GBE0 lower link speed LED	O	CMOS 3.3V

Pin	Signal Name	Description	I/O	I/O Level
P22	GBE0_LED_1000	GBE0 maximum link speed LED	O	CMOS 3.3V
P34	SD2_CMD	SDIO Command/Response	I/O	CMOS 1.8/3.3V
P36	SD2_CLK	SDIO Clock	I/O	CMOS 1.8/3.3V
P39-P42	SD2_DATA0-3	SDIO Data lines	I/O	CMOS 1.8/3.3V
P43	SPI4_SS0	SPI4 Master Chip Select 0	O	CMOS 1.8V
P44	SPI4_SCLK	SPI4 Clock	O	CMOS 1.8V
P54	GPIO5_10/XSPI_SS0	XSPI Master Chip Select 0	O	CMOS 1.8V
P56	GPIO5_09/XSPI_SCLK	XSPI Clock	O	CMOS 1.8V
P60/P61	USB1_DP / USB1_DN	USB Differential Data Pairs Port 1	I/O	USB
P72	ENET_MDC	Management bus clock signal for Ethernet	O	CMOS 1.8V
P73	ENET_MDIO	Management bus data signal for Ethernet	I/O	CMOS 1.8V
P83/P84	PCIe1_CLK_P/N	PCIe1 reference clock output	O	PCIe
P86/P87	PCIe1_RX0_P/N	PCIe1 receive data pair	I	PCIe
P89/P90	PCIe1_TX0_P/N	PCIe1 transmit data pair	O	PCIe
P92-P102	HDMI_TX[0-2]_P/N, TXC_P/N	HDMI Differential Data/Clock Lines	O	TMDS HDMI
P104	HDMI_HPD	HDMI Hot Plug Active High	I	OD LVTTL 5V
P121	I2C4_SCL	I2C4 bus CLK	O	OD CMOS 1.8V
P122	I2C4_SDA	I2C4 bus SDA	I/O	OD CMOS 1.8V
P123-P125	BOOT_MODE0-2	Module boot device straps	I	CMOS 1.8V
P126	RESET_OUT_B	General purpose reset output, active low	O	OD CMOS
P127	RESET_IN_B	Module Reset input, active low	I	OD CMOS
P128	ONOFF_B	Power-button input, active low	I	OD CMOS 1.8V
P143/P144	CAN3_TX / CAN3_RX	CAN3 Transmit/Receive	O/I	CMOS 1.8V
P145/P146	CAN5_TX / CAN5_RX	CAN5 Transmit/Receive	O/I	CMOS 1.8V
P147-P156	VMAIN	Module power input	Analog	3.0-5.25V
S1/S2	I2C3_SCL / I2C3_SDA	I2C3 bus CLK/SDA	I/O	OD CMOS 1.8V
S5	I2C1_SCL	I2C1 bus CLK	I/O	OD CMOS 1.8V
S17-S27	GBE1_TRX*	GBE1 Differential Pair Signals	I/O	GBE MDI
S39-S42	SAI1_TXFS/TXD/RXD/TXC	I2S1 Digital Audio Interface	I/O	CMOS 1.8V
S62-S69	USB2_TX/RX, DP/DN	USB3.0 SuperSpeed + USB2.0 Port 2	O/I	USB SS/USB
S84/S85	PCIe2_CLK_P/N	PCIe2 reference clock output	O	PCIe
S87/S88	PCIe2_RX0_P/N	PCIe2 receive data pair	I	PCIe
S90/S91	PCIe2_TX0_P/N	PCIe2 transmit data pair	O	PCIe
S107	GPIO1_08/LVDS_BL_PWEN	LVDS1 Backlight Enable	O	CMOS 1.8V
S108/S109	LVDS1_CLK_P/N	LVDS1 Differential Pair Clock Lines	O	LVDS
S111-S121	LVDS1_TX0-3_P/N	LVDS1 Differential Pair Data Lines	O	LVDS
S125-S138	DSI/LVDS0_TX0-3, CLK	MIPI DSI / LVDS0 Data and Clock	O	D-PHY/LVDS
S145	WDOG1_OUTPUT_B	Watchdog-Timer Output, active low	O	CMOS 1.8V

Pin	Signal Name	Description	I/O	I/O Level
S147	LI_CELL	Low current RTC backup power	Analog	2~3.25V
S153	SYSTEM_STBY_B	Module Standby State Output	O	OD CMOS
S156	BATLOW_B/GPIO2_12/WIFI_CK	Battery low / 32.768KHz Output	O	CMOS 1.8V
P1	SMB_ALT_B/GPIO5_06/BT_RESET	SMBus Interrupt Signal	I	CMOS 1.8V
P3/P4	CSI1_CKP / CSI1_CKN	CSI1 differential clock input	I	D-PHY
P5	ETH1_1588PPS_OUT	IEEE 1588 Trigger Signal	O	CMOS 1.8V
P7/P8	CSI1_DP0 / CSI1_DN0	CSI1 differential input	I	D-PHY
P10/P11	CSI1_DP1 / CSI1_DN1	CSI1 differential input	I	D-PHY
P13/P14	CSI1_DP2 / CSI1_DN2	CSI1 differential input	I	D-PHY
P16/P17	CSI1_DP3 / CSI1_DN3	CSI1 differential input	I	D-PHY
P19/P20	GBE0_TRXN3 / TRXP3	GBE0 Differential Pair Signals	I/O	GBE MDI
P21	GBE0_LED_10_100	GBE0 lower link speed LED	O	CMOS 3.3V
P22	GBE0_LED_1000	GBE0 maximum link speed LED	O	CMOS 3.3V
P34	SD2_CMD	SDIO Command/Response	I/O	CMOS 1.8/3.3V
P36	SD2_CLK	SDIO Clock	I/O	CMOS 1.8/3.3V
P39-P42	SD2_DATA0-3	SDIO Data lines	I/O	CMOS 1.8/3.3V
P43	SPI4_SS0	SPI4 Master Chip Select 0	O	CMOS 1.8V
P44	SPI4_SCLK	SPI4 Clock	O	CMOS 1.8V
P54	GPIO5_10/XSPI_SS0	XSPI Master Chip Select 0	O	CMOS 1.8V
P56	GPIO5_09/XSPI_SCLK	XSPI Clock	O	CMOS 1.8V
P60/P61	USB1_DP / USB1_DN	USB Differential Data Pairs Port 1	I/O	USB
P72	ENET_MDC	Management bus clock signal for Ethernet	O	CMOS 1.8V
P73	ENET_MDIO	Management bus data signal for Ethernet	I/O	CMOS 1.8V
P83/P84	PCIe1_CLK_P/N	PCIe1 reference clock output	O	PCIe
P86/P87	PCIe1_RX0_P/N	PCIe1 receive data pair	I	PCIe
P89/P90	PCIe1_TX0_P/N	PCIe1 transmit data pair	O	PCIe
P92-P102	HDMI_TX[0-2]_P/N, TXC_P/N	HDMI Differential Data/Clock Lines	O	TMDS HDMI
P104	HDMI_HPD	HDMI Hot Plug Active High	I	OD LVTTL 5V
P121	I2C4_SCL	I2C4 bus CLK	O	OD CMOS 1.8V
P122	I2C4_SDA	I2C4 bus SDA	I/O	OD CMOS 1.8V
P123-P125	BOOT_MODE0-2	Module boot device straps	I	CMOS 1.8V
P126	RESET_OUT_B	General purpose reset output, active low	O	OD CMOS
P127	RESET_IN_B	Module Reset input, active low	I	OD CMOS
P128	ONOFF_B	Power-button input, active low	I	OD CMOS 1.8V
P143/P144	CAN3_TX / CAN3_RX	CAN3 Transmit/Receive	O/I	CMOS 1.8V
P145/P146	CAN5_TX / CAN5_RX	CAN5 Transmit/Receive	O/I	CMOS 1.8V
P147-P156	VMAIN	Module power input	Analog	3.0-5.25V
S1/S2	I2C3_SCL / I2C3_SDA	I2C3 bus CLK/SDA	I/O	OD CMOS 1.8V

Pin	Signal Name	Description	I/O	I/O Level
S5	I2C1_SCL	I2C1 bus CLK	I/O	OD CMOS 1.8V
S17-S27	GBE1_TRX*	GBE1 Differential Pair Signals	I/O	GBE MDI
S39-S42	SAI1_TXFS/TXD/RXD/TXC	I2S1 Digital Audio Interface	I/O	CMOS 1.8V
S62-S69	USB2_TX/RX, DP/DN	USB3.0 SuperSpeed + USB2.0 Port 2	O/I	USB SS/USB
S84/S85	PCIe2_CLK_P/N	PCIe2 reference clock output	O	PCIe
S87/S88	PCIe2_RX0_P/N	PCIe2 receive data pair	I	PCIe
S90/S91	PCIe2_TX0_P/N	PCIe2 transmit data pair	O	PCIe
S107	GPIO1_08/LVDS_BL_PWEN	LVDS1 Backlight Enable	O	CMOS 1.8V
S108/S109	LVDS1_CLK_P/N	LVDS1 Differential Pair Clock Lines	O	LVDS
S111-S121	LVDS1_TX0-3_P/N	LVDS1 Differential Pair Data Lines	O	LVDS
S125-S138	DSI/LVDS0_TX0-3, CLK	MIPI DSI / LVDS0 Data and Clock	O	D-PHY/LVDS
S145	WDOG1_OUTPUT_B	Watchdog-Timer Output, active low	O	CMOS 1.8V
S147	LI_CELL	Low current RTC backup power	Analog	2~3.25V
S153	SYSTEM_STBY_B	Module Standby State Output	O	OD CMOS
S156	BATLOW_B/GPIO2_12/WIFI_CK	Battery low / 32.768KHz Output	O	CMOS 1.8V
P1	SMB_ALT_B/GPIO5_06/BT_RESET	SMBus Interrupt Signal	I	CMOS 1.8V
P3/P4	CSI1_CKP / CSI1_CKN	CSI1 differential clock input	I	D-PHY
P5	ETH1_1588PPS_OUT	IEEE 1588 Trigger Signal	O	CMOS 1.8V
P7/P8	CSI1_DP0 / CSI1_DN0	CSI1 differential input	I	D-PHY
P10/P11	CSI1_DP1 / CSI1_DN1	CSI1 differential input	I	D-PHY
P13/P14	CSI1_DP2 / CSI1_DN2	CSI1 differential input	I	D-PHY
P16/P17	CSI1_DP3 / CSI1_DN3	CSI1 differential input	I	D-PHY
P19/P20	GBE0_TRXN3 / TRXP3	GBE0 Differential Pair Signals	I/O	GBE MDI
P21	GBE0_LED_10_100	GBE0 lower link speed LED	O	CMOS 3.3V
P22	GBE0_LED_1000	GBE0 maximum link speed LED	O	CMOS 3.3V
P34	SD2_CMD	SDIO Command/Response	I/O	CMOS 1.8/3.3V
P36	SD2_CLK	SDIO Clock	I/O	CMOS 1.8/3.3V
P39-P42	SD2_DATA0-3	SDIO Data lines	I/O	CMOS 1.8/3.3V
P43	SPI4_SS0	SPI4 Master Chip Select 0	O	CMOS 1.8V
P44	SPI4_SCLK	SPI4 Clock	O	CMOS 1.8V
P54	GPIO5_10/XSPI_SS0	XSPI Master Chip Select 0	O	CMOS 1.8V
P56	GPIO5_09/XSPI_SCLK	XSPI Clock	O	CMOS 1.8V
P60/P61	USB1_DP / USB1_DN	USB Differential Data Pairs Port 1	I/O	USB
P72	ENET_MDC	Management bus clock signal for Ethernet	O	CMOS 1.8V
P73	ENET_MDIO	Management bus data signal for Ethernet	I/O	CMOS 1.8V
P83/P84	PCIe1_CLK_P/N	PCIe1 reference clock output	O	PCIe
P86/P87	PCIe1_RX0_P/N	PCIe1 receive data pair	I	PCIe
P89/P90	PCIe1_TX0_P/N	PCIe1 transmit data pair	O	PCIe
P92-P102	HDMI_TX[0-2]_P/N, TXC_P/N	HDMI Differential Data/Clock Lines	O	TMDS HDMI
P104	HDMI_HPD	HDMI Hot Plug Active High	I	OD LVTTL 5V

Pin	Signal Name	Description	I/O	I/O Level
P121	I2C4_SCL	I2C4 bus CLK	O	OD CMOS 1.8V
P122	I2C4_SDA	I2C4 bus SDA	I/O	OD CMOS 1.8V
P123-P125	BOOT_MODE0-2	Module boot device straps	I	CMOS 1.8V
P126	RESET_OUT_B	General purpose reset output, active low	O	OD CMOS
P127	RESET_IN_B	Module Reset input, active low	I	OD CMOS
P128	ONOFF_B	Power-button input, active low	I	OD CMOS 1.8V
P143/P144	CAN3_TX / CAN3_RX	CAN3 Transmit/Receive	O/I	CMOS 1.8V
P145/P146	CAN5_TX / CAN5_RX	CAN5 Transmit/Receive	O/I	CMOS 1.8V
P147-P156	VMAIN	Module power input	Analog	3.0-5.25V
S1/S2	I2C3_SCL / I2C3_SDA	I2C3 bus CLK/SDA	I/O	OD CMOS 1.8V
S5	I2C1_SCL	I2C1 bus CLK	I/O	OD CMOS 1.8V
S17-S27	GBE1_TRX*	GBE1 Differential Pair Signals	I/O	GBE MDI
S39-S42	SAI1_TXFS/TXD/RXD/TXC	I2S1 Digital Audio Interface	I/O	CMOS 1.8V
S62-S69	USB2_TX/RX, DP/DN	USB3.0 SuperSpeed + USB2.0 Port 2	O/I	USB SS/USB
S84/S85	PCIe2_CLK_P/N	PCIe2 reference clock output	O	PCIe
S87/S88	PCIe2_RX0_P/N	PCIe2 receive data pair	I	PCIe
S90/S91	PCIe2_TX0_P/N	PCIe2 transmit data pair	O	PCIe
S107	GPIO1_08/LVDS_BL_PWEN	LVDS1 Backlight Enable	O	CMOS 1.8V
S108/S109	LVDS1_CLK_P/N	LVDS1 Differential Pair Clock Lines	O	LVDS
S111-S121	LVDS1_TX0-3_P/N	LVDS1 Differential Pair Data Lines	O	LVDS
S125-S138	DSI/LVDS0_TX0-3, CLK	MIPI DSI / LVDS0 Data and Clock	O	D-PHY/LVDS
S145	WDOG1_OUTPUT_B	Watchdog-Timer Output, active low	O	CMOS 1.8V
S147	LI_CELL	Low current RTC backup power	Analog	2~3.25V
S153	SYSTEM_STBY_B	Module Standby State Output	O	OD CMOS
S156	BATLOW_B/GPIO2_12/WIFI_CK	Battery low / 32.768KHz Output	O	CMOS 1.8V
P1	SMB_ALT_B/GPIO5_06/BT_RESET	SMBus Interrupt Signal	I	CMOS 1.8V
P3/P4	CSI1_CKP / CSI1_CKN	CSI1 differential clock input	I	D-PHY
P5	ETH1_1588PPS_OUT	IEEE 1588 Trigger Signal	O	CMOS 1.8V
P7/P8	CSI1_DP0 / CSI1_DN0	CSI1 differential input	I	D-PHY
P10/P11	CSI1_DP1 / CSI1_DN1	CSI1 differential input	I	D-PHY
P13/P14	CSI1_DP2 / CSI1_DN2	CSI1 differential input	I	D-PHY
P16/P17	CSI1_DP3 / CSI1_DN3	CSI1 differential input	I	D-PHY
P19/P20	GBE0_TRXN3 / TRXP3	GBE0 Differential Pair Signals	I/O	GBE MDI
P21	GBE0_LED_10_100	GBE0 lower link speed LED	O	CMOS 3.3V
P22	GBE0_LED_1000	GBE0 maximum link speed LED	O	CMOS 3.3V
P34	SD2_CMD	SDIO Command/Response	I/O	CMOS 1.8/3.3V
P36	SD2_CLK	SDIO Clock	I/O	CMOS 1.8/3.3V
P39-P42	SD2_DATA0-3	SDIO Data lines	I/O	CMOS 1.8/3.3V
P43	SPI4_SS0	SPI4 Master Chip Select 0	O	CMOS 1.8V

Pin	Signal Name	Description	I/O	I/O Level
P44	SPI4_SCLK	SPI4 Clock	O	CMOS 1.8V
P54	GPIO5_10/XSPI_SS0	XSPI Master Chip Select 0	O	CMOS 1.8V
P56	GPIO5_09/XSPI_SCLK	XSPI Clock	O	CMOS 1.8V
P60/P61	USB1_DP / USB1_DN	USB Differential Data Pairs Port 1	I/O	USB
P72	ENET_MDC	Management bus clock signal for Ethernet	O	CMOS 1.8V
P73	ENET_MDIO	Management bus data signal for Ethernet	I/O	CMOS 1.8V
P83/P84	PCIe1_CLK_P/N	PCIe1 reference clock output	O	PCIe
P86/P87	PCIe1_RX0_P/N	PCIe1 receive data pair	I	PCIe
P89/P90	PCIe1_TX0_P/N	PCIe1 transmit data pair	O	PCIe
P92-P102	HDMI_TX[0-2]_P/N, TXC_P/N	HDMI Differential Data/Clock Lines	O	TMDS HDMI
P104	HDMI_HPD	HDMI Hot Plug Active High	I	OD LVTTL 5V
P121	I2C4_SCL	I2C4 bus CLK	O	OD CMOS 1.8V
P122	I2C4_SDA	I2C4 bus SDA	I/O	OD CMOS 1.8V
P123-P125	BOOT_MODE0-2	Module boot device straps	I	CMOS 1.8V
P126	RESET_OUT_B	General purpose reset output, active low	O	OD CMOS
P127	RESET_IN_B	Module Reset input, active low	I	OD CMOS
P128	ONOFF_B	Power-button input, active low	I	OD CMOS 1.8V
P143/P144	CAN3_TX / CAN3_RX	CAN3 Transmit/Receive	O/I	CMOS 1.8V
P145/P146	CAN5_TX / CAN5_RX	CAN5 Transmit/Receive	O/I	CMOS 1.8V
P147-P156	VMAIN	Module power input	Analog	3.0-5.25V
S1/S2	I2C3_SCL / I2C3_SDA	I2C3 bus CLK/SDA	I/O	OD CMOS 1.8V
S5	I2C1_SCL	I2C1 bus CLK	I/O	OD CMOS 1.8V
S17-S27	GBE1_TRX*	GBE1 Differential Pair Signals	I/O	GBE MDI
S39-S42	SAI1_TXFS/TXD/RXD/TXC	I2S1 Digital Audio Interface	I/O	CMOS 1.8V
S62-S69	USB2_TX/RX, DP/DN	USB3.0 SuperSpeed + USB2.0 Port 2	O/I	USB SS/USB
S84/S85	PCIe2_CLK_P/N	PCIe2 reference clock output	O	PCIe
S87/S88	PCIe2_RX0_P/N	PCIe2 receive data pair	I	PCIe
S90/S91	PCIe2_TX0_P/N	PCIe2 transmit data pair	O	PCIe
S107	GPIO1_08/LVDS_BL_PWEN	LVDS1 Backlight Enable	O	CMOS 1.8V
S108/S109	LVDS1_CLK_P/N	LVDS1 Differential Pair Clock Lines	O	LVDS
S111-S121	LVDS1_TX0-3_P/N	LVDS1 Differential Pair Data Lines	O	LVDS
S125-S138	DSI/LVDS0_TX0-3, CLK	MIPI DSI / LVDS0 Data and Clock	O	D-PHY/LVDS
S145	WDOG1_OUTPUT_B	Watchdog-Timer Output, active low	O	CMOS 1.8V
S147	LI_CELL	Low current RTC backup power	Analog	2~3.25V
S153	SYSTEM_STBY_B	Module Standby State Output	O	OD CMOS
S156	BATLOW_B/GPIO2_12/WIFI_CK	Battery low / 32.768KHz Output	O	CMOS 1.8V

Chapter 3
Software Setup

This chapter describes the procedures for installing or updating firmware on the RM-N95 module. These operations are intended for advanced users familiar with SMARC carrier boards and NXP programming utilities.

Available methods:

- Firmware installation via USB
- Firmware installation via microSD Card

Sections:

- Firmware Installation via USB
  - Entering Download Mode
  - Flashing the Yocto Image
- Firmware Installation via microSD Card
  - Booting from the SD Card
  - Upgrading Firmware via USB Flash Drive

3.1 Firmware Installation via USB

This method allows you to program the RM-N95 module's eMMC storage directly using a host PC. Use this approach for full OS image flashing (Yocto).

⚠ Warning
Firmware installation will erase all data on the eMMC. Ensure stable power and correct cable connections before proceeding.

3.1.1 Entering Download Mode

1) Connect the host PC to the RM-N95 Type-C USB port using a USB cable.

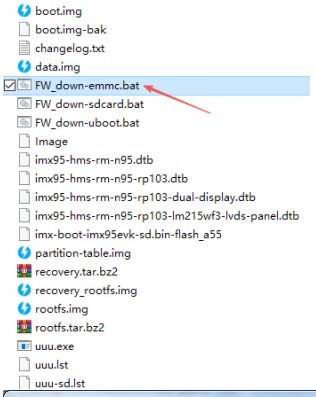
2) On the RM-N95 module, set **SW1** to **1–4: OFF**, **2–3: ON**.

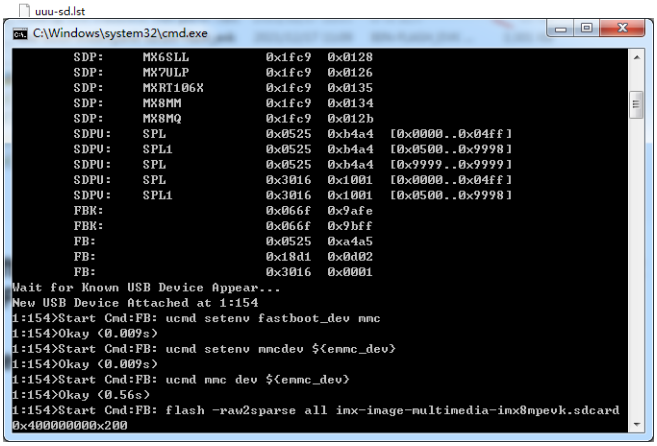
3) On the RP-113 carrier board, set **SW1** to **1-8: OFF**, **2-7: OFF**, **3-6: OFF**, **4-5: OFF**.

4) Power on the carrier board.
5) The system will boot into **Download Mode**.

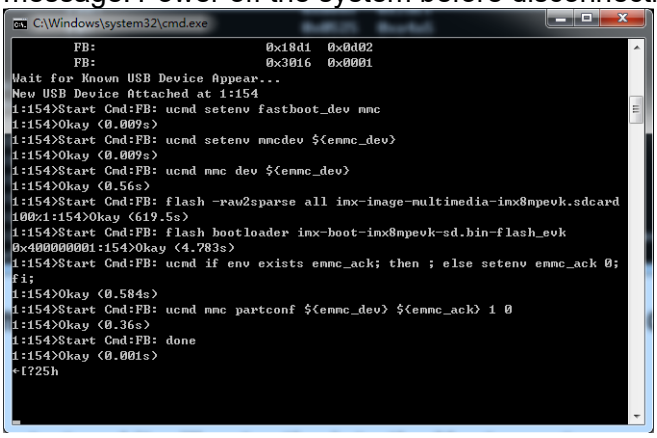
3.1.2 Flashing the Yocto Image

1) On the host PC, double-click **FW_down-emmc.bat** to begin flashing the firmware image.





2) Wait for the process to complete. When finished, the tool will display a success message. Power off the system before disconnecting cables.



3.2 Firmware Installation via microSD Card

This method is intended for users who have the official IBASE firmware image package.

The RP-113 carrier board is typically pre-loaded with an OS (Yocto) in the eMMC.
If recovery or re-installation is required, follow the steps below to prepare and use a recovery microSD Card.

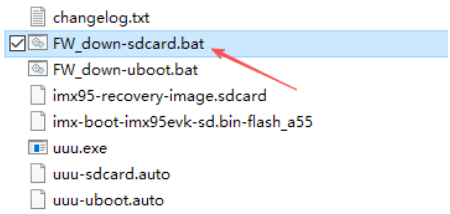
⚠ **Note: All data in the eMMC will be permanently erased.**

System requirements:
- Operating System: Windows 7 or later
- Tool: NXP “uuu” (Universal Update Utility)
- SD Card: 4 GB or greater in size

3.2.1 Booting from the SD Card

1) Insert the prepared microSD Card into slot **P3** on the RP-113 carrier board. Connect **RP-113 P25** to the host PC using a USB Type-A-to-Type-C cable. Set the RM-N95 module boot switch SW1 to 1–4: ON, 2–3: ON (SD Boot, Section 2.2).

2) Execute one of the following methods to flash the SD image:
   - From Command Prompt:
   uuu.exe uuu-sdcard.auto
   - Or, double-click **FW_down-sdcard.bat**.

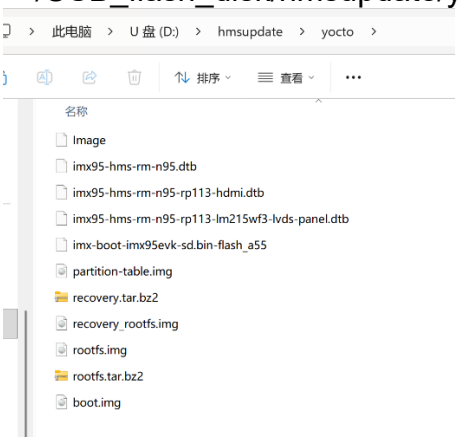


3) Wait for the flashing process to complete before removing power or media.

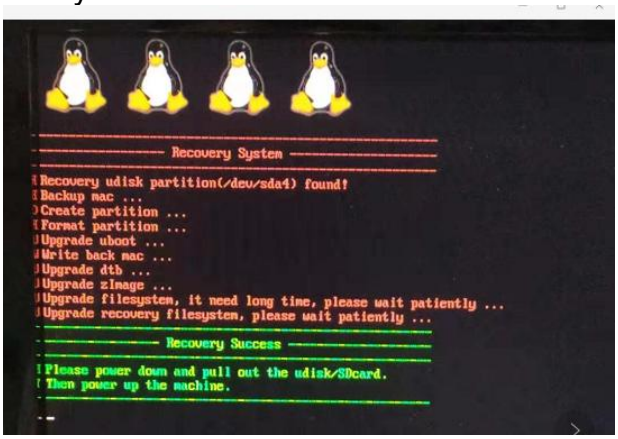
3.2.2 Upgrading Firmware via USB Flash Drive

This method allows you to update the RM-N95 system image using a USB flash drive and recovery microSD Card.

1) Copy the recovery files to a **USB flash drive (FAT32 format)**.
   - For Yocto/Ubuntu images, copy all recovery files to the following directory:
     /USB_flash_disk/hmsupdate/yocto/



2) Insert the **recovery microSD Card** (prepared in Section 3.2.1) into the **RP-113** slot.
3) Insert the **USB flash drive** into the carrier board.
4) Set the DIP switches as follows:
   - **RP-113 SW1:** 1–8 OFF, 2–7 OFF, 3–6 OFF, 4–5 OFF
   - **RM-N95 SW1:** 1–4 ON, 2–3 ON
5) Power on the RP-113 board. The update progress will appear on the HDMI display.
6) When the message **“Flashing successfully completed”** appears, power off the board.
7) Remove the recovery microSD Card and USB flash drive before restarting the system.



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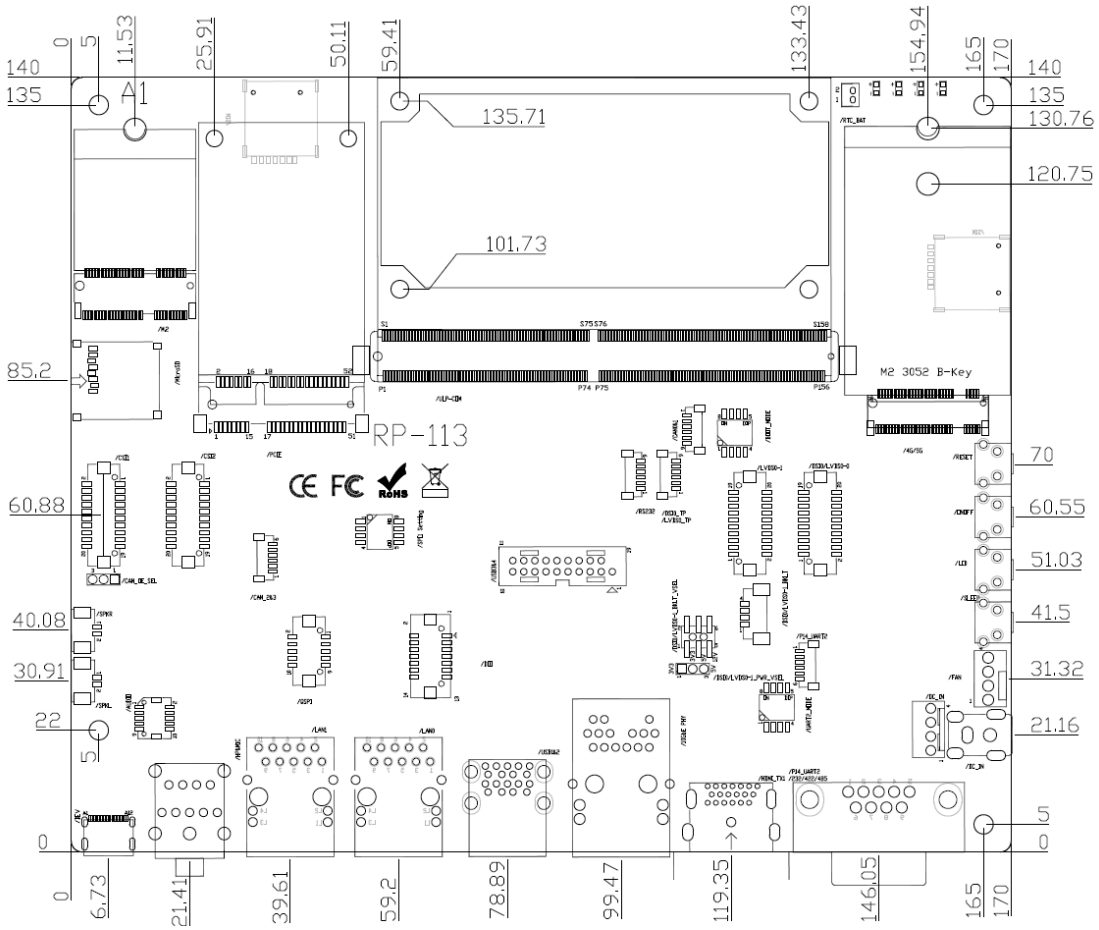
Appendix

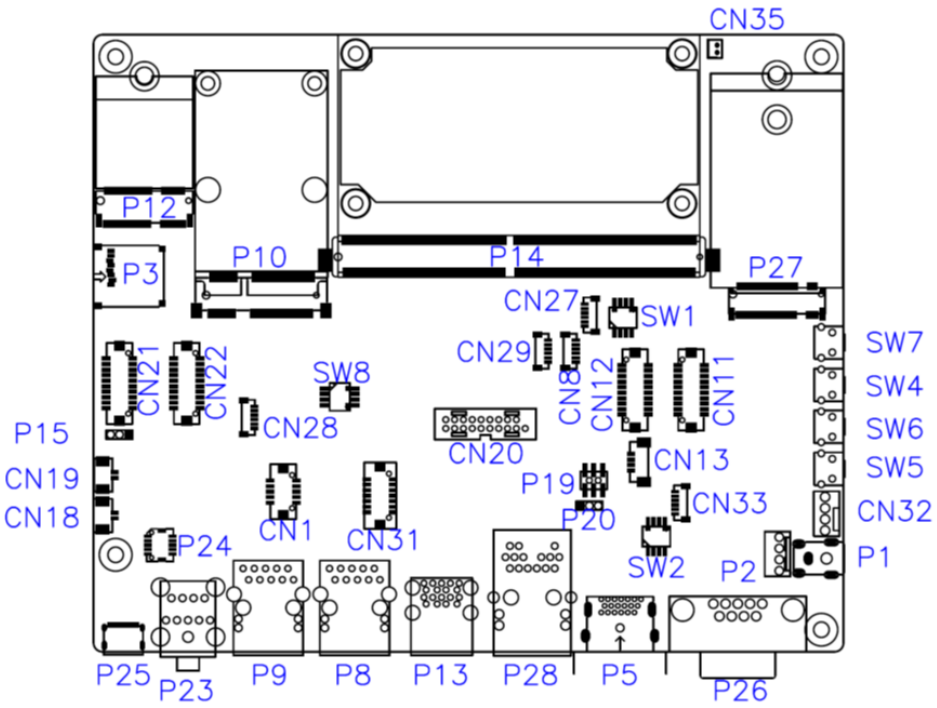
This chapter contains the following information:

RP-113 Dimensions
RP-113 I/O View

A. RP-113 Dimensions



B. RP-113 I/O View



Pin	Assignment	Pin	Assignment
P1	DC-in	CN1	QSPI/XSPI
P2	Internal DC-in	CN6	5G Nano SIM Slot
P3	MicroSD Slot	CN8	DSI0/LVDS0 CTP
P5	HDMI TX1/EDP TX	CN11	DSI0/LVDS0 ch0
P8	GbE LAN0	CN12	LVDS0 ch1
P9	GbE LAN1	CN13	LVDS0 Backlight
P10	mPCIe Slot	CN18	Speaker L
P11	SIM Slot	CN19	Speaker R
P12	M.2 E-Key 2230 Slot	CN20	USB Port 3/4
P13	USB1/2	CN21	MIPI CSI1
P14	MXM3 Slot	CN22	MIPI CSI2
P15	CAN Select	CN27	CAN Port 0/1
P19	DSI0/LVDS0 Backlight Power Select	CN28	CAN Port 2/3
P20	DSI0/LVDS0 LCD Power Select	CN29	COM Port 1/3
P23	Headphone & MIC	CN31	DIO
P24	Line In/Out	CN32	FAN
P25	USB Type-C	CN33	UART(4-wire)
P26	RS232/422/485	CN35	RTC BAT
P27	M.2 B-Key 3042/3052 Slot	SW4	Power ON/OFF Button
P28	10GbE LAN	SW5	Sleep Button
SW1	Boot Mode Select	SW6	LID Button
SW2	UART Mode Select	SW7	Reset Button
SW8	SPI1 Select		